IN THE CLAIMS

Applicant notes that claim 39 was not amended below to overcome prior art but to be correct a typographical error. The amendment made to claim 39 was not narrowing in scope and therefore no prosecution history estoppel arises from the amendment to claim 39. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 U.S.P.Q.2d 1705, 1711-1712 (2002); 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2000). Further, the amendment made to claim 39 was not made for a substantial reason related to patentability and therefore no prosecution history estoppel arises from such an amendment. *See Festo Corp.* at 1707 (2002); *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 41 U.S.P.Q.2d 1865, 1873 (1997).

Claim 1 (original) A method for predicting a result of a conditional branch instruction, comprising the steps of:

determining if a specified condition register field is used to store a branch condition of the conditional branch instruction; and

providing a software branch prediction of the conditional branch instruction as a function of the determination if the specified condition register field is used to store the branch condition of the conditional branch instruction.

Claim 2 (original) The method as recited in claim 1, wherein the software branch prediction predicts that the conditional branch instruction will be taken if the specified condition register field is used to store the branch condition of the conditional branch instruction.

Claim 3 (original) The method as recited in claim 2, wherein the software branch prediction predicts that the conditional branch instruction will be not taken if the specified condition register field is not used to store the branch condition of the conditional branch instruction.

Claim 4 (original) The method as recited in claim 1, wherein the software branch prediction predicts that the conditional branch instruction will be not taken if the specified condition register field is used to store the branch condition of the conditional branch instruction.

Claim 5 (original) The method as recited in claim 4, wherein the software branch prediction predicts that the conditional branch instruction will be taken if the specified condition register field is not used to store the branch condition of the conditional branch instruction.

Claim 6 (original) The method as recited in claim 1, wherein the specified condition register field is N, where N is an integer.

Claim 7 (original) The method as recited in claim 6, wherein the specified condition register field is a multiple of N.

Claim 8 (original) A processor comprising:

an instruction fetch unit for fetching a conditional branch instruction;

circuitry for determining if a specified condition register field is used to store a branch condition of the conditional branch instruction; and

circuitry for providing a software branch prediction of the conditional branch instruction as a function of the determination if the specified condition register field is used to store the branch condition of the conditional branch instruction.

Claim 9 (original) The processor as recited in claim 8, wherein the software branch prediction predicts that the conditional branch instruction will be taken if the specified condition register field is used to store the branch condition of the conditional branch instruction.

Claim 10 (original) The processor as recited in claim 9, wherein the software branch prediction predicts that the conditional branch instruction will be not taken

if the specified condition register field is not used to store the branch condition of the conditional branch instruction.

Claim 11 (original) The processor as recited in claim 8, wherein the software branch prediction predicts that the conditional branch instruction will be not taken if the specified condition register field is used to store the branch condition of the conditional branch instruction.

Claim 12 (original) The processor as recited in claim 11, wherein the software branch prediction predicts that the conditional branch instruction will be taken if the specified condition register field is not used to store the branch condition of the conditional branch instruction.

Claim 13 (original) The processor as recited in claim 8, wherein the specified condition register field is N, where N is an integer.

Claim 14 (original) The processor as recited in claim 13, wherein the specified condition register field is a multiple of N.

Claims 15-38 (withdrawn)

Claim 39 (currently amended) A data processing system for predicting whether a conditional branch instruction will be taken or not taken, the data processing system comprising the program steps of:

determining if the conditional branch instruction [if] is positioned at a specified address in a sequence of instructions being executed; and

predicting whether the conditional branch instruction will be taken or not taken as a function of the position of the specified address.

Claim 40 (original) The data processing system as recited in claim 30, wherein the predicting program step will predict taken if the specified address is a multiple of specified number N.